Abstract of the Invention

An improved DSP processor architecture is presented in which word conditioning (e.g., rounding, saturation, etc.) and analysis operations (e.g., block floating point analysis) are implemented in the write datapath to memory. By moving word conditioning operations from the critical path to the write datapath, the throughput of common DSP functional blocks such as multiplier-accumulator (MAC) blocks may be improved. Delays may be further reduced by combining analysis operations with write or move operations.